PATENT ABSTRACTS OF JAPAN

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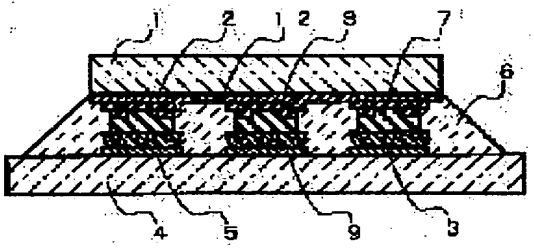
(54) SEMICONDUCTOR DEVICE AND PACKAGING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To solve a problem that conductivity is lowered by decreasing a connection area when connecting wiring formed on a substrate and a bump electrode while using an anisotropic conductive adhesive since the bump electrode to be formed on a semiconductor device is advanced to be made into multi-pin and fine pitch and the bump electrode is reduced with increase in the number of bump electrodes to be formed on the semiconductor device.
SOLUTION: A conductive particle 3 is arranged on bump electrodes 7 formed on the semiconductor device by plating and that semiconductor device is packaged on a substrate 4 formed with wiring 5 through an insulating resin 6 by thermocompression fixing. Thus, flip chip packaging is enabled with sufficient connection resistance in a fine connection area and extremely high insulation between bump electrodes 7 or between wiring 5.



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[Claim(s)]
[Claim 1] The semiconductor device characterized by having the plating film and an electric conduction particle on the projection electrode prepared in the semiconductor device, or an in-and-out force terminal.
[Claim 2] The semiconductor device according to claim 1 obtained by plating by immersing the semiconductor device which equipped the plating liquid containing an electric conduction particle with the projection electrode or the in-and-out force terminal.
[Claim 3] Said electric conduction particle is a semiconductor device according to claim 1 or 2 characterized by being metal particles or the particle which comes to install a metal membrane in the front face of the particle which consists of an insulating material.
[Claim 4] The process which plates by immersing the semiconductor device which equipped the plating liquid containing an electric conduction particle with the projection electrode or the in-and-out force terminal, The process which prepares the substrate in which wiring was formed and installs non-hardened insulating resin on a substrate, The process which performs alignment for wiring of the projection electrode of a semiconductor device or an in-and-out force terminal, and a substrate, The mounting approach of the semiconductor device characterized by having the process which hardens insulating resin, and fixes [which is fixed and electric-flows] the projection electrode of a semiconductor device or an in-and-out force terminal, and wiring of a substrate through an electric conduction particle.
[Claim 5] Said electric conduction particle is the mounting approach of the semiconductor device according to claim 4 characterized by being metal particles or the particle which comes to install a metal membrane in the front face of the particle which consists of an insulating material.

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device in the flip chip mounting approach of mounting a semiconductor device on a direct substrate, and its mounting approach.

[0002]
[Description of the Prior Art] When it carries a semiconductor device in a substrate, the flip chip mounting approach is learned as an approach of connecting the projection electrode on a semiconductor device, and wiring on a substrate. The approach of connecting the projection electrode of a semiconductor device and wiring on a substrate using electric conduction adhesives and the approach of connecting the projection electrode of a semiconductor device and wiring on a substrate to a resin film using the anisotropy electric conduction film which distributed the electric conduction particle are raised to the flip chip mounting approach.
[0003] The sectional view of a part on which the semiconductor device 1 which gave the flip chip mounting approach of having used the anisotropy electric conduction film 11 for drawing 16 , and the substrate 4 were pasted up is shown. The anisotropy electric conduction film 11 is stuck on the substrate 4 in which wiring 5 was formed, alignment of the common electrode 8 and the projection electrode 7 which were formed in the input/output terminal 2 on a semiconductor device 1, and the wiring 5 formed on the substrate 4 is carried out, and it connects by heating and pressurization. Only the electric conduction particle 3 which is between the projection electrode 7 and wiring 5 at this time is crushed, electrical installation with the wiring 5 formed on the substrate 4 is performed, and insulation is maintained in the part which a pressure does not join.
[0004] The mounting approach of the semiconductor device in the conventional technique is explained using drawing 2 - drawing 5 , drawing 14 - drawing 16 . Drawing 2 is the sectional view showing a semiconductor device 1. On the semiconductor device 1, the circuit element (not shown) and the input/output terminal 2 are formed, the protective coat 12 is formed on the circuit element (not shown) and the input/output terminal 2, and opening of the protective coat 12 of input/output terminal 2 part is carried out.
[0005] On the protective coat 12 of the semiconductor device 1 shown in drawing 2 , and an input/output terminal 2, as shown in drawing 3 , the common electrode layer 8 is formed. Although the formation approach of the common electrode layer 8 forms metal membranes, such as aluminum, chromium, copper, titanium, and a tungsten, with the sputtering method or vacuum evaporation technique, especially a metaled class is not limited.
[0006] The resist 10 which consists of a photopolymer is applied on a semiconductor device 1, as shown in drawing 4 , and it patternizes so

that opening of the resist 10 of the part which forms the input/output terminal 2 top 7, i.e., a projection electrode, by exposure development may be carried out. The common electrode 8 is used as cathode by this, by performing electrolytic plating, as shown in drawing 5 , plating grows up to be only opening of a resist and the projection electrode 7 can be formed in it. The projection electrode 7 formed at this time can be formed with metals, such as gold, copper, nickel, and a pewter.

[0007] Then, as shown in drawing 14 , a resist 10 is removed, and the common electrode 8 and the projection electrode 7 remain only on an input/output terminal 2 by etching the common electrode 8, as shown in drawing 15 . In case the common electrode 8 is etched, the projection electrode 7 can remove only the common electrode 8 by considering as the metal which is not etched with the metal into which the common electrode 8 is etched, without etching the projection electrode 7. For example, the common electrode 8 is formed with copper, the projection electrode 7 is formed withgold, and only the common electrode 8 exposed by being immersed in a nitric acid or ammonium persulfate is etched.

[0008] By using the anisotropy electric conduction film 11 for the substrate 4 which formed wiring 5 for the semiconductor device 1 which formed the projection electrode 7 as shown in drawing 16 , and mounting by heating and pressurization, the electric conduction particle 3 is caught between the projection electrode 7 and wiring 4, and an electric flow can be obtained.

[0009]

[Problem(s) to be Solved by the Invention] The formation of many pins and detailed pitch-ization are progressing, the number of the projection electrodes formed in a semiconductor device follows the projection electrode formed in a semiconductor device on increasing, a projection electrode also becomes small, in case wiring and the projection electrode which were formed on the substrate are connected using different good electric conduction adhesives, connection area decreases and conductivity falls. The number of the electric conduction particles which exist in connection between a projection electrode and wiring also decreases, so that the connection area of the projection electrode on a semiconductor device and wiring on a substrate becomes detailed, and it becomes difficult to obtain connection resistance low enough.

[0010] For example, in the conventional flip chip mounting, when connection area was made quite small, connection resistance increased rapidly in the projection electrode of a semiconductor device and a semiconductor device was used as an object for the drive of a liquid crystal display, the light-and-darkness difference occurred the whole liquid crystal driver zone of each semiconductor device, and the problem that image quality will deteriorate had arisen.

[0011] In case the purpose of this invention connects the projection electrode formed in the semiconductor device, and wiring formed on the substrate, its insulation with the terminal which is low resistance and adjoins is high, and is to offer the semiconductor device which can connect in a very small area, and its mounting approach.

[0012]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device in this invention and its mounting approach adopt the manufacture approach of the following publication.

[0013] The semiconductor device of this invention is characterized by having the plating film and an electric conduction particle on the projection electrode prepared in the semiconductor device, or an in-and-out force terminal. Moreover, it is characterized by this electric conduction particle being metal particles or a particle which comes to install a metal membrane in the front face of the particle which consists of an insulating material.

[0014] Moreover, this semiconductor device is immersed in the semiconductor device which equipped the plating liquid containing an electric conduction particle with the projection electrode or the in-and-out force terminal, and is characterized by being obtained by plating.

[0015] The process which furthermore plates by immersing the mounting approach of the semiconductor device of this invention in the semiconductor device which equipped the plating liquid containing an electric conduction particle with the projection electrode or the in-and-out force terminal, The process which prepares the substrate in which wiring was formed and installs non-hardened insulating resin on a substrate, It is characterized by having the process which performs alignment for wiring of the projection electrode of a semiconductor device or an in-and-out force terminal, and a substrate, and the process to which insulating resin is hardened, and ****** of a semiconductor device fixes [fix and it electric-flows] an in-and-out force terminal and wiring of a substrate through an electric conduction particle.

[0016]

[Embodiment of the Invention] The sectional view of the mounting structure in the semiconductor device of this invention is shown in drawing 1 . The electric conduction particle 3 exists only in the connection of the projection electrode 7 prepared in the semiconductor device 1, and the wiring 5 prepared on the substrate 4, and it has the

structure where the electric conduction particle 3 does not exist in the other part so that it may indicate to drawing 1 . The electric conduction particle is installed with the plating film 9. Moreover, the projection electrode 7 is not formed and it does not matter as a configuration which installs the electric conduction particle 3 and the plating film in the top face of the in-and-out force terminal 2 which etched the common electrode 8 partially and formed it.

[0017] Since sufficient number to obtain connection resistance of several 10mohm exists, the electric conduction particle 3 which exists in the connection of the projection electrode 2 prepared on the semiconductor device 1 and the wiring 5 prepared on the substrate 4 can obtain connection resistance low enough, even when the connection area of the projection electrode 2 and wiring 5 is very small.

[0018]

[Example] Next, the manufacture approach of the semiconductor device of this invention and the mounting approach are explained using a drawing. Drawing 1 to drawing 13 is the sectional view showing the semiconductor device and its mounting approach of this invention.

[0019] The approach of forming a projection electrode on a semiconductor device can be formed by the same approach as the Prior art shown by drawing 5 from drawing 2 . The quality of the material of the projection electrode 7 used the quality of the material of the projection electrode 7 as gold in this example, although metals, such as gold, copper, and nickel, were raised. Although especially the configuration of the projection electrode 7 asks neither straight Wall nor a mushroom in that case, it is desirable that it is a SUTO rate wall configuration in consideration of applying a pressure to the electric conduction particle 3, and connecting the projection electrode 7 and wiring on a substrate.

[0020] After forming the projection electrode 7 in opening of a resist 10, while the semiconductor device 1 in which the projection electrode 7 was formed is immersed in the plating liquid containing the electric conduction particle 3 and the plating film 9 is deposited on projection electrode 7 front face like drawing 5 , the electric conduction particle 3 is made to adhere, as shown in drawing 6 . The electric conduction particle 3 used at this time uses metal particles, such as gold, silver, copper, and nickel, and a nucleus as plastics or glass, and particle size chooses the particle size optimal in 1 in all-10 micrometers for connection area using the particle which covered the front face by the metal membrane. Although especially the class of plating liquid was not asked, it gold-plated in this example.

[0021] Then, as shown in drawing 7 , a resist 10 is removed, and the common electrode 8 and the projection electrode 7 remain only on an input/output terminal 2 by etching the common electrode 8, as shown in drawing 8 . In case the common electrode 8 is etched, the projection electrode 7 can remove only the common electrode 8 by considering as the metal which is not etched with the metal into which the common electrode 8 is etched, without etching the projection electrode 7. On projection electrode 7 front face formed on the input/output terminal 2 on a semiconductor device 1 as the above-mentioned process showed to drawing 8 , the structure where the electric conduction particle 3 was held with the plating film 9 can be acquired.

[0022] Moreover, as shown in drawing 3 , after forming the common electrode layer 8, the resist 10 which consists of a photopolymer is applied on a semiconductor device 1, as shown in drawing 10 , and it patternizes so that opening of the resist 10 on an input/output terminal 2 may be carried out by exposure development. Under the present circumstances, thickness of a resist 10 is made thinner than the time of forming a projection electrode. And while a semiconductor device 1 is immersed in the plating liquid containing the electric conduction particle 3 and the plating film 9 is deposited on the in-and-out force terminal 2 top face, the electric conduction particle 3 is made to adhere, as shown in drawing 11 . The electric conduction particle 3 used at this time can reach, and plating liquid can use a thing equivalent to the ingredient indicated previously.

[0023] Then, as shown in drawing 12 , a resist 10 is removed, and the common electrode 8 remains only on an input/output terminal 2 by etching the common electrode 8, as shown in drawing 13 . The structure where the electric conduction particle 3 was held with the plating film 9 on the input/output terminal 2 of a semiconductor device 1 as the above-mentioned process showed to drawing 13 can be acquired. Thus, the projection electrode 2 may not be formed on the input/output terminal of a semiconductor device 1, but the electric conduction particle 3 and the plating film 9 may be arranged on the in-and-out force terminal 2.

[0024] The following process is explained using drawing 9 . Wiring 5 is formed with the sputtering method, vacuum evaporation technique, plating, etc. on a substrate 4, etching performs pattern NINGU, and the substrate in which wiring was formed is prepared. On the substrate 4 which formed wiring 5, the shape of a film and liquefied insulating resin 6 are arranged, and temporary attachment is performed by liquefied or carrying out alignment and pushing the projection

electrode 2 and the electric conduction particle 3 which were prepared on the semiconductor device 1 of drawing 8 , and the wiring 5 prepared on the substrate 4 so that it may illustrate to drawing 9 .
[0025] What added the amine system, the acid-anhydride system, and the imidazole system curing agent to epoxy base resin, such as the bisphenol A mold, a bisphenol female mold, and a novolak mold, as insulating resin 6 can be used. Moreover, it is what mixed fillers, such as carbon, and a calcium carbonate, a silica, and the thing in which additives, such as a reaction accelerator and a plasticizer, were made to mix depending on the case may be used.
[0026] Then, electrical installation is performed for the projection electrode 7 and wiring 5 through the electric conduction particle 3 at the same time it stiffens closure resin with a thermocompression bonding fixture (not shown). this time -- between the projection electrode 7 and wiring 5 -- several 10 -- since a sufficient number for obtaining connection resistance of m ohm of electric conduction particles 3 exist and the electric conduction particle 3 does not exist other than a connection part -- [0027] in which flip chip mounting with very high sufficient connection resistance in a very small connection area and insulation during the wiring 4 between the projection electrodes 2 is possible Thus, the semiconductor device of this invention was able to be mounted on the substrate like drawing 1 . Here, the plating film and the semiconductor device of drawing 13 equipped with 9 electric-conduction particle 3 may be used on the in-and-out force terminal 2 instead of the semiconductor device of drawing 8 which formed the projection electrode 7 as a semiconductor device 1.
[0028] The electric conduction particle 3 exists only in the connection of the projection electrode 2 prepared in the semiconductor device 1, and the wiring 5 prepared on the substrate 4, and it has the structure where the electric conduction particle 3 does not exist in the other part so that it may illustrate to drawing 1 . Since sufficient number to obtain connection resistance of several 10mohm existed, the electric conduction particle 3 which exists in the connection of the projection electrode 2 prepared on the semiconductor device 1 and the wiring 5 prepared on the substrate 4 was able to obtain connection resistance low enough, even when the connection area of the projection electrode 2 and wiring 5 was very small.
[0029]
[Effect of the Invention] Flip chip mounting to which an electric-conduction particle is arranged, many electric-conduction particles exist only in the connection of a projection electrode and wiring, and an electric-conduction particle does not exist from plating on the projection electrode formed on the semiconductor device other than a connection by mounting the semiconductor device in the substrate in_which wiring was formed, by thermocompression bonding through insulating resin so that clearly from the above explanation and which it has in low connection resistance and high insulation is obtained.
[0030] Moreover, even when the connection area of the projection electrode or in-and-out force terminal formed on the semiconductor device, and wiring formed on the substrate is very small, a sufficient number for the connection of electric conduction particles can be arranged, and high-density connection is attained.

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the semi-conductor mounting approach of this invention.
[Drawing 2] It is the sectional view showing the formation approach of the conventional projection electrode.
[Drawing 3] It is the sectional view showing the formation approach of the conventional projection electrode.
[Drawing 4] It is the sectional view showing the formation approach of the conventional projection electrode.
[Drawing 5] It is the sectional view showing the formation approach of the conventional projection electrode.
[Drawing 6] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 7] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 8] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 9] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 10] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 11] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 12] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 13] It is the sectional view showing the mounting approach of the semiconductor device of this invention.
[Drawing 14] It is the sectional view showing the formation approach of the conventional projection

electrode.

[Drawing 15] It is the sectional view showing the formation approach of the conventional projection electrode.

[Drawing 16] It is the sectional view showing the mounting approach of the conventional semiconductor device.

[Description of Notations]

1 Semiconductor Device
2 In-and-out Force Terminal
3 Electric Conduction Particle
4 Substrate
5 Wiring
6 Insulating Resin
7 Projection Electrode
8 Common Electrode
9 Plating Film
10 Resist
11 Anisotropy Electric Conduction Film

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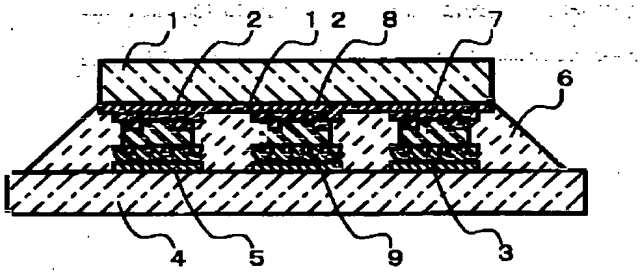
(54)【発明の名称】　半導体装置とその実装方法

(57)【要約】
【課題】　半導体装置に形成する突起電極は多ピン化、微細ピッチ化が進んでおり、半導体装置に形成する突起電極の数が増加するに伴い、突起電極も小さくなり、基板上に形成した配線と突起電極とを異方正導電接着剤を用いて接続する際、接続面積が減少し、導電性が低下する。
【解決手段】　半導体装置上に形成した突起電極７上に、メッキ法より導電粒子３を配置し、その半導体装置を配線５を形成した基板４に絶縁樹脂６を介して熱圧着によって実装することで、微少な接続面積での十分な接続抵抗と、突起電極７間または配線５間の絶縁性が非常に高いフリップチップ実装が可能である



【特許請求の範囲】
【請求項１】　半導体装置に設けられた突起電極上あるいは出入力端子上に、メッキ膜と導電粒子とを備えたことを特徴とする半導体装置。
【請求項２】　導電粒子を含有したメッキ液に、突起電極あるいは出入力端子を備えた半導体装置を浸漬し、メッキを行うことによって得られた請求項１に記載の半導体装置。
【請求項３】　前記導電粒子は金属粒子、または絶縁物よりなる粒子の表面に金属膜を設置してなる粒子であることを特徴とする請求項１又は請求項２に記載の半導体装置。
【請求項４】　導電粒子を含有したメッキ液に、突起電極あるいは出入力端子を備えた半導体装置を浸漬し、メッキを行う工程と、配線を形成した基板を用意し、基板上に未硬化の絶縁樹脂を設置する工程と、半導体装置の突起電極あるいは出入力端子と基板の配線とを位置合わせを行う工程と、絶縁樹脂を硬化し、半導体装置の突起電極あるいは出入力端子と基板の配線とを、導電粒子を介して電気的導通および固定する工程を有することを特徴とする半導体装置の実装方法。
【請求項５】　前記導電粒子は金属粒子、または絶縁物よりなる粒子の表面に金属膜を設置してなる粒子であることを特徴とする請求項４に記載の半導体装置の実装方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は半導体装置を直接基板上に実装するフリップチップ実装方法における半導体装置とその実装方法に関するものである。
【０００２】
【従来の技術】半導体装置を基板に搭載する場合、半導体装置上の突起電極と基板上の配線とを接続する方法として、フリップチップ実装方法が知られている。フリップチップ実装方法には、導電接着剤を用いて半導体装置の突起電極と基板上の配線とを接続する方法と、樹脂フィルムに導電粒子を分散させた異方性導電膜を用いて半導体装置の突起電極と基板上の配線とを接続する方法があげられる。
【０００３】図１６に異方性導電膜１１を用いたフリップチップ実装方法を施した半導体装置１と基板４とを接着した部分の断面図を示す。配線５を形成した基板４上に異方性導電膜１１を張り付け、半導体装置１上の入出力端子２に形成した共通電極８および突起電極７と、基板４上に形成した配線５とを位置合わせし、加熱、加圧により接続を行う。このとき突起電極７と配線５の間にある導電粒子３だけが潰れ、基板４上に形成した配線５との電気的接続が行われ、圧力が加わらない部分では絶縁性が保たれる。
【０００４】図２～図５、図１４～図１６を用いて従来技術における半導体装置の実装方法について説明する。図２は半導体装置１を示す断面図である。半導体装置１上には回路素子（図示せず）と入出力端子２が設けてあり、保護膜１２が回路素子（図示せず）および入出力端子２上に形成してあり、入出力端子２部分の保護膜１２は開口している。
【０００５】図２に示す半導体装置１の保護膜１２と入出力端子２上に、図３に示すように共通電極膜８を形成する。共通電極膜８の形成方法はスパッタリング法や真空蒸着法によりアルミニウム、クロム、銅、チタン、タングステンなどの金属膜を形成するが、金属の種類は特に限定されない。
【０００６】感光性樹脂からなるレジスト１０を図４に示すように半導体装置１上に塗布し、露光現像により入出力端子２上すなわち突起電極７を形成する部分のレジスト１０を開口するようパターン化する。これにより共通電極８を陰極とし、電解メッキを行うことで、図５に示すようにレジストの開口部にのみ、メッキが成長していき突起電極７を形成することができる。このとき形成する突起電極７は金、銅、ニッケル、ハンダなどの金属で形成することができる。
【０００７】その後、図１４に示すようにレジスト１０を除去し、図１５に示すように共通電極８をエッチングすることにより入出力端子２上のみに共通電極８と突起電極７が残る。共通電極８をエッチングする際に、共通電極８がエッチングされる金属で、突起電極７はエッチングされない金属とすることで突起電極７はエッチングされずに共通電極８のみを除去することができる。たとえば共通電極８を銅で形成し、突起電極７を金で形成しておき、硝酸や過硫酸アンモニウムに浸漬することで露出している共通電極８のみエッチングされる。
【０００８】図１６に示すように突起電極７を形成した半導体装置１を配線５を形成した基板４に異方性導電膜１１を用いて加熱、加圧により実装することで、突起電極７と配線４の間に導電粒子３が挟まり電気的導通を得ることができる。
【０００９】
【発明が解決しようとする課題】半導体装置に形成する突起電極は多ピン化、微細ピッチ化が進んでおり、半導体装置に形成する突起電極の数が増加するに伴い、突起電極も小さくなり、基板上に形成した配線と突起電極とを異方正導電接着剤を用いて接続する際、接続面積が減少し、導電性が低下する。半導体装置上の突起電極と基板上の配線との接続面積が微細になっていくほど接続に突起電極と配線の間に存在する導電粒子の数も減少していき、十分に低い接続抵抗を得ることが難しくなる。
【００１０】たとえば、従来のフリップチップ実装では、接続面積をかなり小さくすると、半導体装置の突起電極において接続抵抗値が急増し、液晶表示装置の駆動用として半導体装置を用いた場合には、各半導体装置の

液晶駆動領域ごとで明暗差が発生し、画像品質が低下してしまうという問題が生じていた。

【００１１】本発明の目的は、半導体装置に形成した突起電極と基板上に形成した配線とを接続する際に、低抵抗でかつ隣接する端子との絶縁性が高く、微少な面積で接続が行える半導体装置とその実装方法を提供することにある。

【００１２】

【課題を解決するための手段】上記の目的を達成するために、本発明における半導体装置とその実装方法は下記記載の製造方法を採用する。

【００１３】本発明の半導体装置は、半導体装置に設けられた突起電極上あるいは出入力端子上に、メッキ膜と導電粒子とを備えたことを特徴としている。またこの導電粒子は金属粒子、または絶縁物よりなる粒子の表面に金属膜を設置してなる粒子であることを特徴としている。

【００１４】また、この半導体装置は、導電粒子を含有したメッキ液に、突起電極あるいは出入力端子を備えた半導体装置を浸漬し、メッキを行うことによって得られることを特徴としている。

【００１５】さらに本発明の半導体装置の実装方法は、導電粒子を含有したメッキ液に、突起電極あるいは出入力端子を備えた半導体装置を浸漬し、メッキを行う工程と、配線を形成した基板を用意し、基板上に未硬化の絶縁樹脂を設置する工程と、半導体装置の突起電極あるいは出入力端子と基板の配線とを位置合わせを行う工程と、絶縁樹脂を硬化し、半導体装置の突起電共あるいは出入力端子と基板の配線とを、導電粒子を介して電気的導通および固定する工程を有することを特徴としている。

【００１６】

【発明の実施の形態】図１に本発明の半導体装置における実装構造の断面図を示す。図１に記載するように、半導体装置１に設けた突起電極７と、基板４上に設けた配線５との接続部にのみ導電粒子３が存在し、それ以外の部分には導電粒子３が存在しない構造となっている。導電粒子はメッキ膜９と共に設置されている。また、突起電極７を設けず、共通電極８を部分的にエッチングして形成した出入力端子２の上面に導電粒子３とメッキ膜を設置する構成としても構わない。

【００１７】半導体装置１上に設けた突起電極２と基板４上に設けた配線５との接続部に存在する導電粒子３は数１０mΩの接続抵抗を得るのに十分な数が存在しているので、突起電極２と配線５との接続面積が微少な場合でも十分に低い接続抵抗を得ることができる。

【００１８】

【実施例】次に本発明の半導体装置の製造方法と実装方法を図面を用いて説明する。図１から図１３は、本発明の半導体装置およびその実装方法を示す断面図である。

【００１９】半導体装置上に突起電極を形成する方法は、図２から図５までに示した従来の技術と同じ方法で形成することができる。突起電極７の材質は金、銅、ニッケルなどの金属があげられるが、本実施例では突起電極７の材質を金とした。その際、突起電極７の形状はストレートウォールやマッシュルームなど特に問わないが、導電粒子３に圧力を加えて突起電極７と、基板上の配線とを接続することを考慮し、ストーレートウォール形状であることが望ましい。

【００２０】図５のように、レジスト１０の開口部に突起電極７を形成した後、導電粒子３を含有したメッキ液に突起電極７を形成した半導体装置１を浸漬し、突起電極７表面にメッキ膜９を析出させると同時に、導電粒子３を図６に示すように付着させる。この時使用する導電粒子３は金、銀、銅、ニッケルなどの金属粒子や、核をプラスチックまたはガラスとし、表面を金属膜で覆った粒子を用い、粒径は接続面積に合わせて１～１０μmの範囲で最適な粒径を選択する。メッキ液の種類は特に問わないが、本実施例では金メッキを施した。

【００２１】その後、図７に示すようにレジスト１０を除去し、図８に示すように共通電極８をエッチングすることにより入出力端子２上のみに共通電極８と突起電極７が残る。共通電極８をエッチングする際に、共通電極８がエッチングされる金属で、突起電極７はエッチングされない金属とすることで突起電極７はエッチングされずに共通電極８のみを除去することができる。上記工程により図８に示すように半導体装置１上の入出力端子２上に形成した突起電極７表面に、導電粒子３がメッキ膜９により保持された構造を得ることができる。

【００２２】また、図３に示すように共通電極膜８を形成した後、感光性樹脂からなるレジスト１０を図１０に示すように半導体装置１上に塗布し、露光現像により入出力端子２上のレジスト１０を開口するようパターン化する。この際、突起電極を形成した時よりも、レジスト１０の膜厚は薄くする。そして、導電粒子３を含有したメッキ液に半導体装置１を浸漬し、出入力端子２上面にメッキ膜９を析出させると同時に、導電粒子３を図１１に示すように付着させる。この時使用する導電粒子３はおよびメッキ液は先に記載した材料と同等のものを使用することができる。

【００２３】その後、図１２に示すようにレジスト１０を除去し、図１３に示すように共通電極８をエッチングすることにより入出力端子２上のみに共通電極８が残る。上記工程により図１３に示すように半導体装置１の入出力端子２上に、導電粒子３がメッキ膜９により保持された構造を得ることができる。このように半導体装置１の入出力端子上に突起電極２は形成せず、出入力端子２上に導電粒子３とメッキ膜９を配置してもかまわない。

【００２４】次の工程を図９を用いて説明する。基板４

上にスパッタリング法、真空蒸着法、メッキ法などで配線５を設け、エッチングによりパターンニングを行い、配線を形成した基板を用意する。配線５を設けた基板４上に液状またはフィルム状または液状の絶縁樹脂６を配置し、図８の半導体装置１上に設けた突起電極２および導電粒子３と、基板４上に設けた配線５とを、図９に図示するように位置合わせし、押しつけることで仮付けを行う。

【００２５】絶縁樹脂６としてはビスフェノールＡ型、ビスフェノールＦ型、ノボラック型などのエポキシ主剤にアミン系、酸無水物系、イミダゾール系硬化剤を加えたものなどが使用できる。またカーボンや炭酸カルシウム、シリカなどのフィラーを混入したもので、場合によっては、反応促進剤、可塑剤などの添加剤を混入させたものを使用してもかまわない。

【００２６】その後、熱圧着治具（図示せず）によって封止樹脂を硬化させると同時に、突起電極７と配線５とを導電粒子３を介して電気的接続を行う。この時、突起電極７と配線５との間には数１０ｍΩの接続抵抗を得るための十分な数の導電粒子３が存在し、接続部分以外には導電粒子３が存在しないため、微少な接続面積での十分な接続抵抗と、突起電極２間または配線４間の絶縁性が非常に高いフリップチップ実装が可能である

【００２７】このようにして、図１のように本発明の半導体装置を基板上に実装することができた。ここで、半導体装置１として突起電極７を形成した図８の半導体装置の代わりに、出入力端子２上にメッキ膜と９導電粒子３を備えた図１３の半導体装置を用いてもかまわない。

【００２８】図１に図示するように、半導体装置１に設けた突起電極２と基板４上に設けた配線５との接続部にのみ、導電粒子３が存在し、それ以外の部分には導電粒子３が存在しない構造となっている。半導体装置１上に設けた突起電極２と基板４上に設けた配線５との接続部に存在する導電粒子３は数１０ｍΩの接続抵抗を得るのに十分な数が存在しているので、突起電極２と配線５との接続面積が微少な場合でも十分に低い接続抵抗を得ることができた。

【００２９】

【発明の効果】以上の説明から明らかなように、半導体装置上に形成した突起電極上に、メッキ法より導電粒子を配置し、その半導体装置を配線を形成した基板に絶縁樹脂を介して熱圧着によって実装することで、突起電極と配線との接続部にのみ導電粒子が多く存在し、接続部以外には導電粒子が存在しない、低い接続抵抗と高い絶縁性を兼ね備えたフリップチップ実装が得られる。

【００３０】また、半導体装置上に形成した突起電極あるいは出入力端子と、基板上に形成した配線との接続面積が微少な場合でも、その接続部に十分な数の導電粒子を配置することができ、高密度な接続が可能となる。

【図面の簡単な説明】

【図１】本発明の半導体実装方法を示す断面図である。

【図２】従来の突起電極の形成方法を示す断面図である。

【図３】従来の突起電極の形成方法を示す断面図である。

【図４】従来の突起電極の形成方法を示す断面図である。

【図５】従来の突起電極の形成方法を示す断面図である。

【図６】本発明の半導体装置の実装方法を示す断面図である。

【図７】本発明の半導体装置の実装方法を示す断面図である。

【図８】本発明の半導体装置の実装方法を示す断面図である。

【図９】本発明の半導体装置の実装方法を示す断面図である。

【図１０】本発明の半導体装置の実装方法を示す断面図である。

【図１１】本発明の半導体装置の実装方法を示す断面図である。

【図１２】本発明の半導体装置の実装方法を示す断面図である。

【図１３】本発明の半導体装置の実装方法を示す断面図である。

【図１４】従来の突起電極の形成方法を示す断面図である。

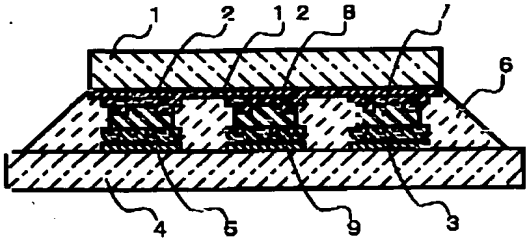
【図１５】従来の突起電極の形成方法を示す断面図である。

【図１６】従来の半導体装置の実装方法を示す断面図である。

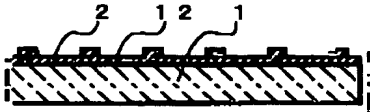
【符号の説明】

１　半導体装置
２　出入力端子
３　導電粒子
４　基板
５　配線
６　絶縁樹脂
７　突起電極
８　共通電極
９　メッキ膜
１０　レジスト
１１　異方性導電膜

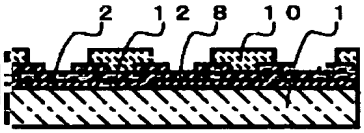
【図1】



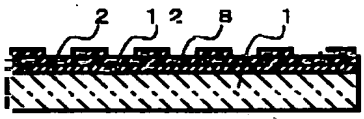
【図2】



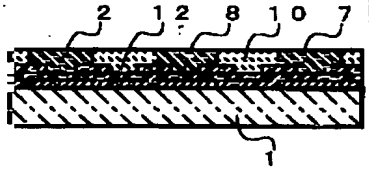
【図4】



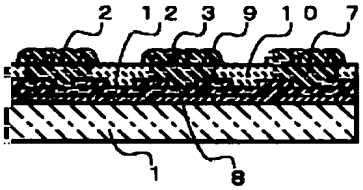
【図3】



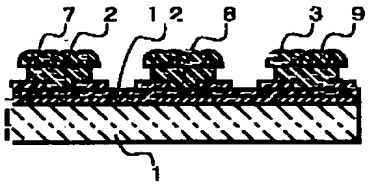
【図5】



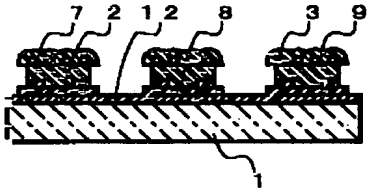
【図6】



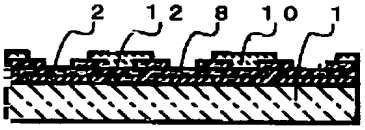
【図7】



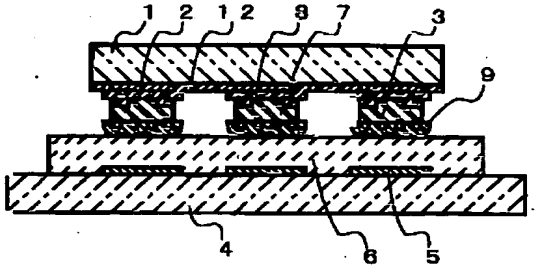
【図8】



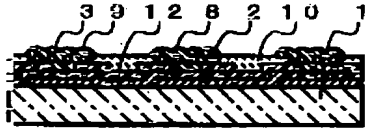
【図10】



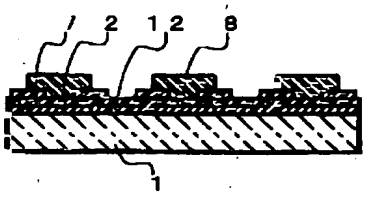
【図9】



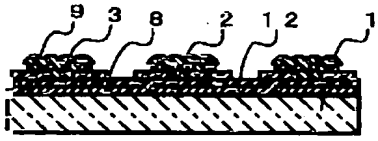
【図11】



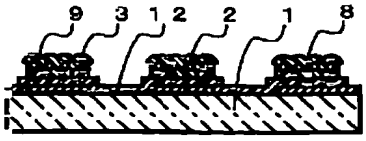
【図14】



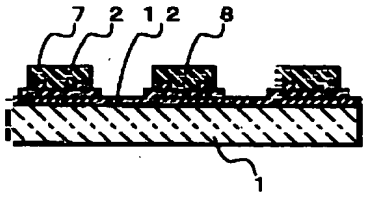
【図12】



【図13】



【図15】



【図16】